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A Novel High Gain Ultra Wide Band Receiver for 3.1 – 10.6 GHz Frequency

Upkar
M.TECH Student
E.C.E D, N.I.U
Greater Noida, U.P.

Mr. Owais Shah
Assistant Professor
E.C.E.D, N.I.U
Greater Noida, U.P.

Dharmendra Kumar Sharma
Assistant Professor
E.E.D, IIMT College
Greater Noida, U.P.

ABSTRACT:
Ultra-Wideband (UWB) technologies are widely accepted as the center piece of wireless interconnects for next generation Wireless Personal Area Networks (WPAN). It finds great applications in high-connectivity and high interoperability multimedia consumer products within personal operating space, such as wireless home video distributions systems, high-speed, high-mobility cable replacement solution, such as Wireless Universal Serial Bus (W-USB) and Fire wire. Currently different types of academic and industrial work are going on the implementation of UWB monolithic transceivers. This work focuses on system and circuit co-design of a fully integrated CMOS LNA and mixer, with emphasis on architectural issue and circuit topologies of its Novel high gain. In this work a new design of an Ultra-wideband (UWB) Low noise Amplifier (LNA), Mixer and receiver are proposed using 0.13 µm CMOS technology and simulated using Cadence "Virtuoso" tools so that its operate at the range of 3.1 to 10.6 GHz. In this design, specific architecture has been selected for LNA and Mixer implementation of an Ultra-wideband communication system. The basic architecture of the LNA designed herein exhibits a resistive feedback amplifier followed by a differential pair with input and output impedance matching circuits. It will help to reduce the number of expensive space consuming passive inductors which will minimize the chip area. The design will also minimize the Noise figure of the circuit and power consumption. It will improve the circuit gain. The LNA and Mixer achieved a maximum gain of 17 dB and Noise figure reduces to a minimum level of 1.96 dB over the band of 3.1-10.6 GHz. The power consumption of the circuit is reduced to 12 mw because of better impedance matching circuit available in the implemented design. The overall Gain of 17 dB and Noise figure from 2.7 to 3.5 dB is proposed for the complete receiver circuit over the band of 3.1 to 10.6 GHz as desired.

KEYWORDS: LNA, MIXER, GAIN, UWB, CMOS, Frequency

INTRODUCTION:

A Novel High Gain Ultra Wideband receiver is designed and simulated using 0.13 µm CMOS process with the help of Virtuoso VLSI tools. The novel high gain, consisting of LNA and Mixer is designed to operate over a wideband of frequencies (3.1-10.6 GHz). The implemented LNA consists of two cascaded amplifier stages. The design and implementation of the circuit in particular architecture exhibits an extra ordinary performance, which is preferable for an operating network. The LNA and Mixer maintain maximum Gain up to 16.2 dB, Noise figure 1.76 dB and power consumption of 12 mw respectively which is comparatively better than previous works. The Novel High Gain (LNA) achieves the maximum Gain up to 17.2 dB at the frequency range 4 to 5 GHz, the minimum Noise figure is reduced up to 2.6 dB for frequency range 4.5 to 5.5 GHz, and Power consumption is reduced to 12 mw for the band width of 3.1 – 10.6 GHz. Therefore by using these results, we can implement a new Ultra Wideband receiver, which can be used in modern day communication system (WiMAX & LTE) to operate with a modulating Gain, Noise figure, impedance matching and lower power requirements for a wide range of frequency.

Still the design can be further modified to obtain higher speed of operations and wider range of frequency, so that it can be implemented in any UWB communication system, which will minimize the losses, chip area and power consumptions with improved performances.

IMPLEMENTED DIAGRAM OF NOVEL HIGH GAIN ULTRA WIDE BAND RECEIVER:

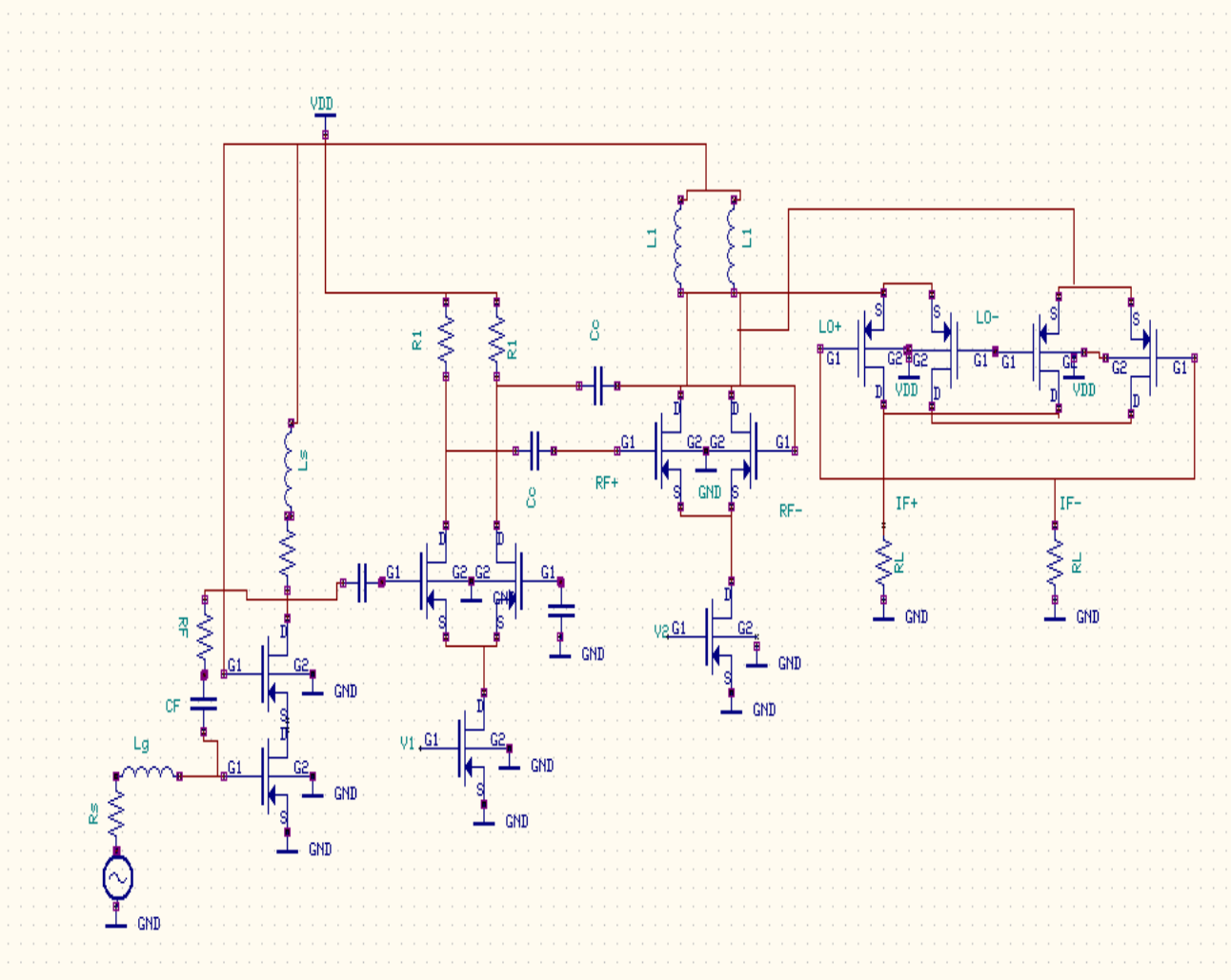

Figure 1 Novel High Gain Receivers

LNA and mixer have been separately analyzed and discussed in the thesis sections. A LNA designs and a mixer topologies have been proposed and simulated. However, it is necessary to integrate them as a high gain design for the direct conversion receiver, so that the novel system performance can be verified. The schematic of the circuits are shown in Figure 1 To interface the LNA and mixer, ac coupling capacitors are used. The low frequency second order nonlinear products and dc-offset from the LNA will be blocked by the coupling capacitors.

SIMULATION RESULTS OF THE CIRCUITS:

This work demonstrates that a low-power, high performance UWB LNA and Mixer can be realized using 0.13-μm CMOS technology.

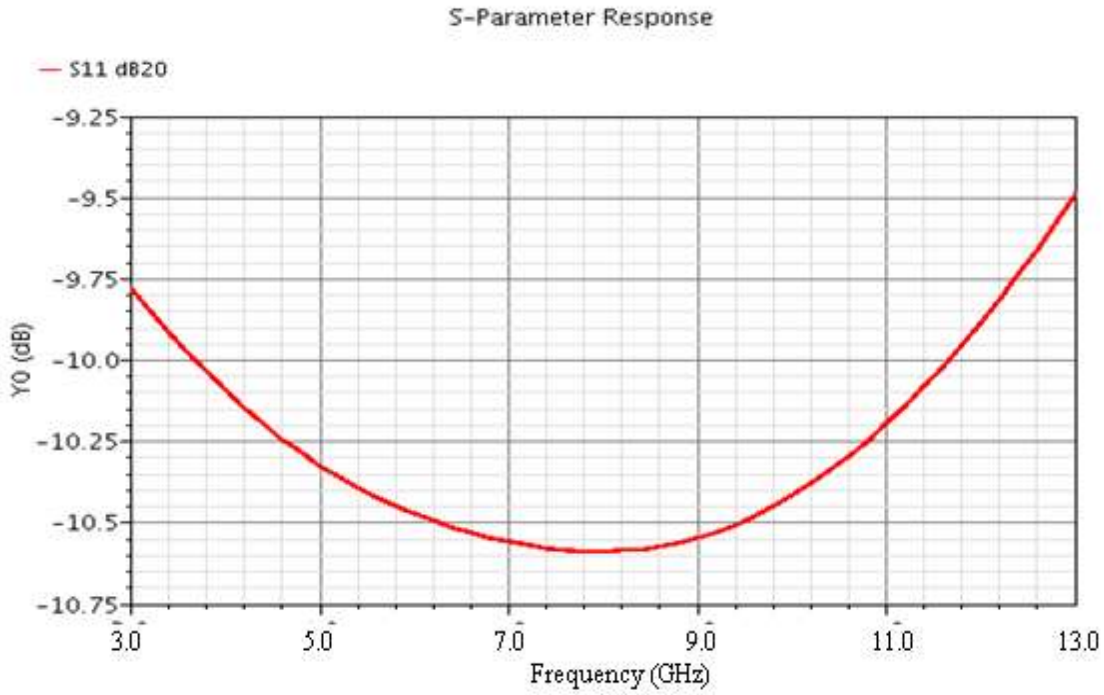

Figure 2.1 S_{11} of Novel High Gain Receiver

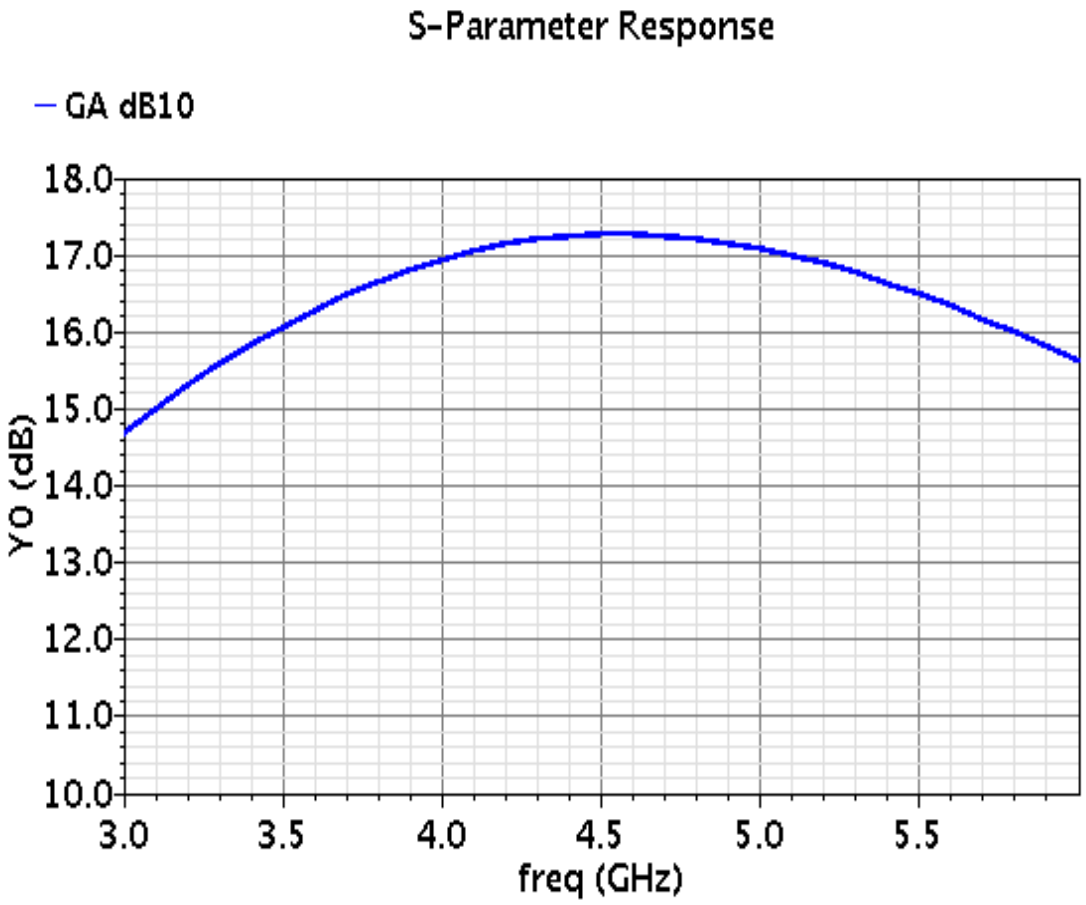

Figure 2.2 Gain of Novel High Gain Receiver

The simulated results of the proposed Novel High Gain Receiver are presented in Figure 2.1 to Figure 2.4. In this simulation results, the Noise figure and Voltage Gain of the Novel High Gain is 1.96 dB and 16.2 dB respectively. Due to power mismatch at integration point higher gain cannot be achieved. This result shows that the noise figure of the Novel High Gain is still kept below 2 dB even when there is a drastic change in its gain.

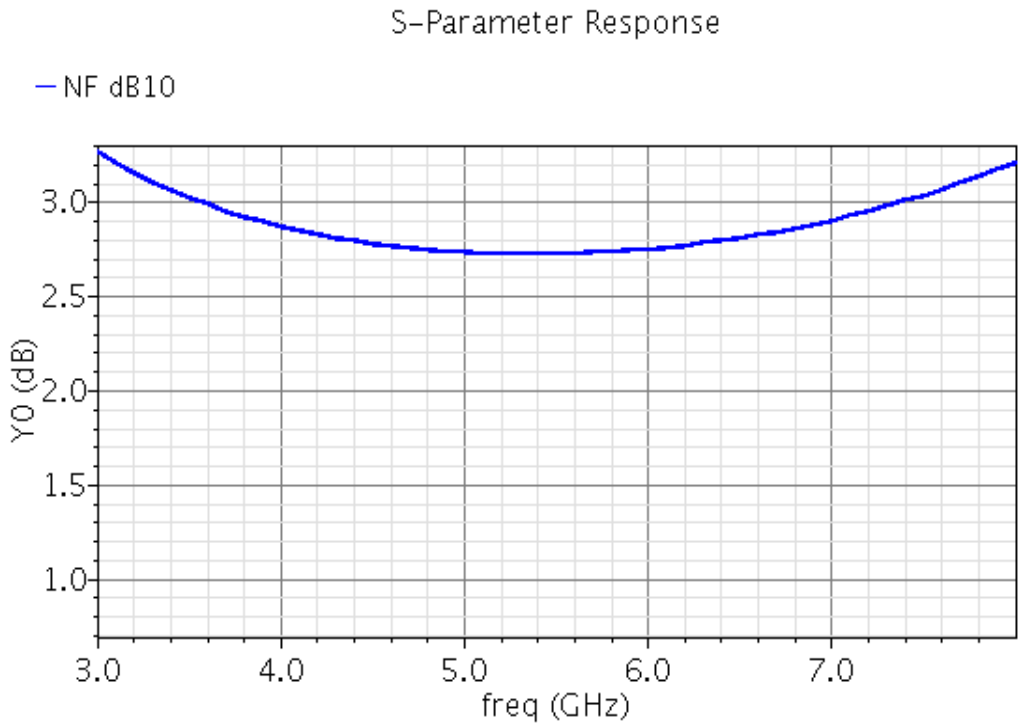

Figure 2.3 Noise Figure of Novel High Gain Receiver

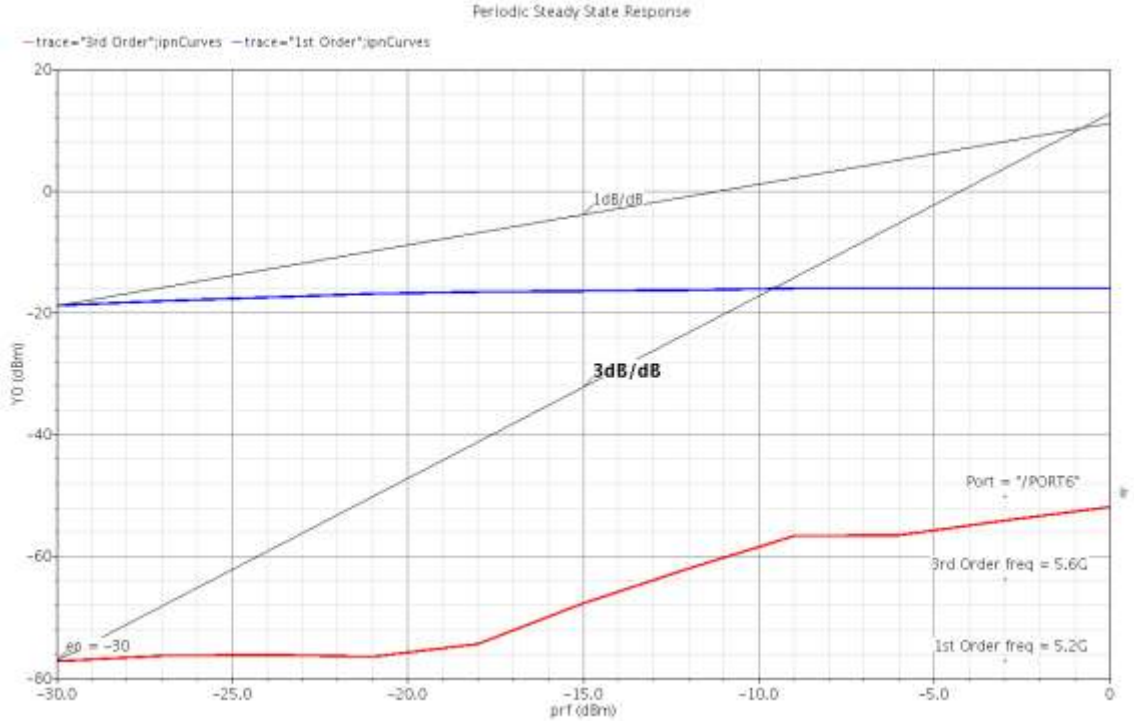

Figure 2.4 IIP3 of Novel High Gain Receiver

LAYOUT CONSIDERATIONS:

In a high frequency design, the layout of a circuit plays a very important role. This is because layout determines the nature of parasitic resistances and capacitance which can alter the performance of the circuit dramatically. Signal strength at the LNA input is so small that it can easily be corrupted by the substrate noise, adjacent on-chip high power signals and interferences (clocks etc). Under these circumstances, a good layout practice becomes very essential. The most critical devices are placed quite close to each other to achieve good matching and at the same time maintaining good isolation from each other. Due to better modeling for higher frequencies, MOSFETs from the design library are used. Since these devices have fixed encapsulated layout, techniques such as inter-digitization become difficult to realize. Hence in order to improve matching, MOSFETs are placed closed to each other in such a way that process variations on either axis of orientation result in the lowest mismatch. Layout of the UWB LNA is shown in Figure As seen in the layout, transistor are laid along y axis such that process variation on x axis have little effect on the transistor and process variations on y axis will be same on both the transistors leading to better matching. Another major concern for LNAs is the series resistance of interconnects. Keeping this in mind, top metal layer is used for interconnection and multiple metal to metal contacts are used in parallel to reduce overall interconnect resistance. In this layout most of area is acquired by capacitor and inductor. We have not taken blocking capacitor in this layout.

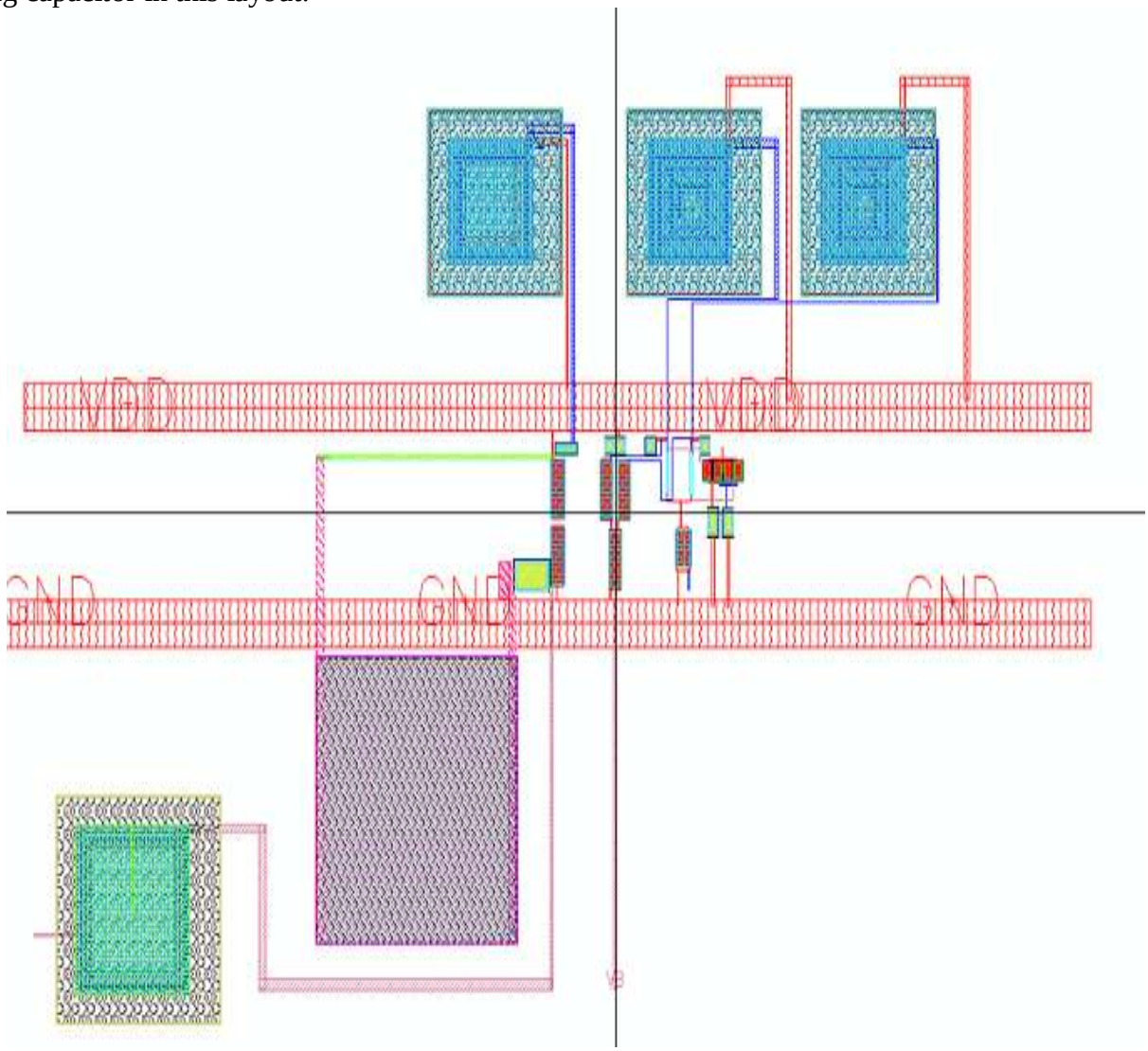

Figure Layout of Novel High Gain Receive

CONCLUSIONS:

The entitled work's conclusion is as-

1. The RF Front end is implemented and Simulated with the help of 0.13 µm CMOS technology for Ultra Wide Band frequency.
2. The Power consumption is reduced up to 12 mw for 3.1 to 10.6 GHz frequency.
3. The Front end gain is improved up to 17.2 dB for the frequency range 3.5 – 6 GHz, and remains above 15 dB over the range of frequency 3.1 – 10.6 GHz.
4. The Noise Figure is reduced up to 2.6 dB for the frequency range 3.1 – 10.6 GHz.

REFERENCES:-

1. Bevilacqua A. "An Ultra Wide band CMOS Low-Noise Amplifier for 3.1- 10.6-GHz Wireless Receivers," IEEE Journal of Solid-State Circuits, (2011), 39, P. 2259.
2. Jiseon P. "A 3-5 GHz RF Receiver Front-End for UWB Wireless System" Microwave Conf. of IEEE, (2010), 36, P. 1511
3. Liao C. "A broadband noise canceling CMOS LNA for 3.1–10.6-GHz UWB receiver", IEEE Journal of Solid State Circuit Conference, (2009), 42, P. 329.
4. Lin Y. "A 3.1–10.6 GHz Ultra-wideband CMOS low noise amplifier with current-reused technique", IEEE MWC Letters, (2010), 17, P. 232.
5. Gharpurey R. "A Broadband Low-Noise Front-End Amplifier for UWB in 0.13um CMOS", Proc. of IEEE Conference on Custom Integrated Circuits, (2009), P. 605 .
6. Michael T. "A 1.2 V reactive-feedback 3.1– 10.6 GHz LNA in .13 µm CMOS", IEEE Journal of Solid-State Circuits, (2007), 42, P. 1023.
7. Sviteket R. "DC offsets in direct conversion receivers: characterization and implications", IEEE Microwave Mag., (2005), 6, P. 76.
8. Darabi H. "Noise in RF- CMOS Mixers: A Simple Physical Model," IEEE Journal of Solid-State Circuits, (2005), 15, P. 35.
9. Hayderi P. et. al, "Design and analysis of an ultra wideband distributed CMOS mixer," IEEE Trans. VLSI Systems, (2005), 13 , P. 618.
10 Delang F."A 0.18µm CMOS high linearity flat conversion gain down-conversion mixer for UWB receiver" IEEE conference of Solid State Integrated Circuit, (2008), P. 1492.
11 Safarian A. et. al, "Designing and analysis of Ultra Wide band distributed CMOS mixer" IEEE transaction on VLSI, (2005) , 13, P. 618.
12 Lanka N. et. al, "Frequency hopped Quadrature Frequency synthesizer in 0.13 µ m technology" IEEE Journal of Solid State, (2011) , 46, P. 2021.
13 Shaeffer D. et. al, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier," IEEE Journal of Solid-State Circuits, (2004), 32, P. 745.
14 Hayderi P. et. al., "Design of CMOS distributed circuit for multiband wireless UWB receivers," IEEE conference of RFIC, (2011), P. 695.